Design of Chaotic and Hyperchaotic Time-Delayed Electronic Circuit

Tanmoy Banerjee, Debabrata Biswas and B.C. Sarkar

Abstract--- *The present paper reports a first order nonlinear retarded type time-delayed chaotic and hyperchaotic electronic circuit. The proposed circuit has three distinct advantages over the existing time-delayed circuits. First, it has a nonlinearity that is expressed by closed form mathematical functions, which makes the analysis and design of the circuit easier. Second, the time-delay part of the proposed circuit is realized with an active All-Pass Filter (APF), in which no inductor is used, and the variation of delay is obtained simply by the variation of a resistor, which is more advantageous than to vary the inductor in LCL delay blocks that is widely used in all the time-delayed circuits existing in the literature. Third, the circuit shows hyperchaos even for a moderate time-delay. We describe the systematic design procedure of the circuit, and whenever necessary, the experimental results are corroborated by the numerical computations. We show that the circuit shows limit cycle oscillation, bifurcation scenario, chaotic and hyperchaotic oscillations.*

Keywords--- *Delay Dynamical System, Chaos, Hyperchaos, Nonlinear Electronic Circuit*

I. INTRODUCTION

DELAY dynamical systems have been grabbing the attention of researchers of various fields including physics, mathematics, biology, economics, engineering, etc. The presence of the delay in a system makes the system infinite dimensional and may lead to an unstable and oscillatory system response. In particular, the presence of a time delay in a nonlinear system may give rise to various complex phenomena like, bifurcation, chaos, hyperchaos, multistability, etc.

A plethora of natural systems are modeled by DDEs; examples include blood production in patients with leukemia (Mackey-Glass model) [1], dynamics of optical systems (e.g., Ikeda system) [2, 3], population dynamics [4], El Niño/southern oscillation (ENSO) [5], the electrodynamics of interacting charged particles (the Lorentz force with Liénard–Weichert potentials) [6], neural networks [7], etc.

Apart from the mathematical modeling of the naturally occurring phenomena, nonlinear delay dynamical systems have been extensively studied in the literature, and several new systems were proposed [8,9] due to the following reasons: (i) owing to the infinite dimensionality, DDEs shows higher dimensional chaotic behavior that cannot be anticipated by a low dimensional system [10]. Understanding and exploring the behavior of these systems are important both from the academic and engineering perspectives, (ii) infinite dimensionality of delayed systems offers a great opportunity to the researchers to harness the richness of hyperchaos, having multiple positive Lyapunov exponents (LEs). It has already been established that communication with a low dimensional chaos (having a single positive LE) is not fully secured because an eavesdropper can reconstruct the chaotic attractor and retrieve the hidden message [11]. Therefore, the synchronization of hyperchaotic systems has been proposed as an alternative method for improving the security in the communication scheme [12]. As a simple time delay system with suitable nonlinearity can produce a hyperchaotic signal with multiple positive LEs, thus they have been identified as good candidates for a secure communication system [13]. Apart from a secure communication system, chaotic and hyperchaotic circuits have important applications in chaos-based noise generators [14]. Due to these reasons, efforts are made to design *simple and well characterized* time delay systems that can produce chaos and hyperchaos [9]. Nonlinear time delayed systems that can be implemented with off-the-shelf electronic circuits are of particular interest due to their application potentiality; that is why many electronic circuits and systems have been reported in the literature [15-25].

In this paper we report the detailed experimental studies of a simple chaotic electronic circuit proposed by the authors in Ref.[9]. The circuit has a single constant time-delay and a closed form mathematical function describing the nonlinearity. The detailed analysis of the circuit has been recently reported in [9], but here in this paper our aim is to explore the experimental aspects of the parametric variation of the circuit behavior. To design the analog delay line, we have used an active all pass filter (APF) as the delay element; in the previous research works reported in [15-23] all the delay blocks were constructed by an LCL filter to produce delay. This causes the output to attenuate when large number of LCL blocks is used to achieve a large delay. Whether in our circuit as we have used the active APF, the attenuation is overcome due the presence of the active element. The output does not depend on the frequency of the signal in the APF, only the phase part of the input signal depends on the signal frequency. Experimental results show that the system shows stable limit cycle, bifurcation scenario, chaos and hyperchaos.

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II. SYSTEM DESCRIPTION

Figure 1 describes schematic of the proposed electronic circuit. The block for nonlinearity is shown by “ND” and the circuit diagram is given in figure 2. From figure 2 we can say the Nonlinear Device has three parts:

1. A diode (D1) which acts as a half wave rectifier having nonlinearity $0.5(|V_\tau| + V_\tau)$;
2. The circuit associated with A_1 op-amp which is an inverting amplifier having gain $\frac{R_2}{R_1}$. The output is a linear function of the input for a certain range of the input voltage; for a higher input voltage, the output is saturated to a constant, $\pm V_{sat}$, which is the saturation voltage of the op-amp. This nature of the op-amp based amplifier can be represented by the following function:

$$-\beta V_{sat} \tanh\left(\omega \frac{R_2}{R_1} \frac{V_\tau}{V_{sat}}\right)$$

where, $V_\tau = V(t - \tau)$, β and ω are the scaling factors needed to fit the model with the experimental data; with a proper choice of the resistor values, one can match the experimental data with the theoretical ‘tanh’ function. In general, for smaller input voltages, $\beta \approx 1$ and $\omega \approx 1$.

3. Finally, of A_2 which acts as a weighted adder.

Thus we can write the following form of the nonlinearity:

$$f(V(t - T_D)) = -\frac{R_5}{R_3} 0.5[|V(t - T_D)| + V(t - T_D)] + \frac{R_5}{R_4} \beta V_{sat} \tanh\left(\omega \frac{R_2}{R_1} \frac{V(t - T_D)}{V_{sat}}\right) \quad (1)$$

The delay part is shown by “Variable τ ” and the circuit diagram is given in figure 3. The variable delay element is realized by a first order All Pass Filter (APF) (Fig. 3) [26]. The APF has the following transfer function

$$T(s) = -a_1 \frac{s - \omega_0}{s + \omega_0} \quad (2)$$

With flat gain $a_1 = 1$ (determined by R_8 and R_9), and $\omega_0 = 1/CR$ is the frequency at which the phase shift is $\pi/2$. Since it has an almost linear phase response, each APF block contributes a delay $T_D \approx RC$. So i blocks produces a delay of $T_D = iRC$ ($i = 1, 2, \dots$). By changing the resistance R , one can vary the amount of delay; thus one can control the resolution of the delay line.

The signal from the nonlinear part of the circuit if fed to an inverting amplifier with gain b (this is a system parameter). Then the resulting signal is passed through a low pass filter (LPF), next the low pass filtered signal is fed to the variable delay circuit through a buffer to match the impedances. The output of the delay block is injected to the nonlinear block through another buffer. The buffers are designed with unity gain non-inverting op-amps. In figure 2, A_1, A_2, A_3 are op-

amps. It gives the required nonlinearity to make the system nonlinear. Figure 3 shows the circuit diagram of the active all pass filter (APF). The R_0 - C_0 section is the low pass filter (LPF). The variable b is a system parameter which can be varied to examine the system behavior. This is actually done by varying the resistance R_7 as shown in figure 2. We can also use the delay term as the system parameter and can vary it by varying the value of the resistance R in figure 3.

Figure 1: Experimental Circuit Diagram. $R_0 = 1 \text{ k}\Omega$, $C_0 = 100 \text{ nF}$. Buffers are Designed with Unity Gain Non-Inverting Operational Amplifiers

Let $V(t)$ be the voltage drop across the capacitor C_0 of the LPF section R_0 - C_0 ; So the equation which represents the time evolution of the circuit is given by:

$$R_0 C_0 \frac{dV(t)}{dt} = -V(t) - bf(V(t - T_D)) \quad (3)$$

Figure 2: Nonlinear Device along with the Amplifying Stage. A_1 - A_3 are op-amps (TL 074), D1 is the diode: 1N4148, $R_1 = 16.55 \text{ k}\Omega$, $R_2 = 20.24 \text{ k}\Omega$, $R_3 = 5.25 \text{ k}\Omega$, $R_4 = 15.05 \text{ k}\Omega$, $R_5 = R_6 = 10 \text{ k}\Omega$.

Here, $b = R_7/R_6$ is the gain of the amplifier A_3 (fig. 2). $f(V(t - T_D)) \equiv f(V_\tau)$ is the nonlinear function representing the output of the Nonlinear Device (ND) of fig. 2 in terms of the input voltage V_τ . T_D is the time delay produced by the delay block.

Let us now define the following dimensionless variables and parameters: $t = \frac{t}{R_0 C_0}$, $\tau = \frac{T_D}{R_0 C_0}$, $x = \frac{V(t)}{V_{sat}}$, $x(t - \tau) = \frac{V(t - T_D)}{V_{sat}}$, $\frac{R_5}{R_3} = n_1$, $\beta \frac{R_5}{R_4} = m_1$, $\omega \frac{R_2}{R_1} = l_1$.

Figure 3: Active First-Order all Pass Filter (APF). $R_8 = R_9 = 2.2 \text{ k}\Omega$, $C = 10 \text{ nF}$.

Now the system equation (1) can be reduced to the following dimensionless first-order, nonlinear delay differential equation given by:

$$\frac{dx}{dt} = -x(t) - bf(x(t-\tau)), \quad (4)$$

where

$$f(x(t-\tau)) \equiv f(x_\tau) = -n_1 0.5(|x_\tau| + x_\tau) + m_1 \tanh(l_1 x_\tau) \quad (5)$$

This function is actually the nonlinearity produced in the ND part of the circuit in Figure 2. Equation (4) is the system equation of our proposed electronic circuit. Figure 4 shows the nature of the nonlinearity of the nonlinear function given by Equation (5) for different sets of the parameters.

III. EXPERIMENTAL RESULTS

The proposed circuit is designed on hardware level on a breadboard using IC TL074 (quad JFET op-amp) with a ± 12 volt power supply. Capacitors have 5% tolerance. For low pass section, we choose $R_0 = 1 \text{ k}\Omega$ and $C_0 = 100 \text{ nF}$. For the nonlinear device (ND), we use a 1N4148 diode; the following resistor values are used: $R_1 = 16.55 \text{ k}\Omega$, $R_2 = 20.24 \text{ k}\Omega$, $R_3 = 5.25 \text{ k}\Omega$, $R_4 = 15.05 \text{ k}\Omega$, $R_5 = 10 \text{ k}\Omega$. Figure 5 shows the experimentally obtained nonlinearity produced by the ND. The gain of the noninverting amplifier A_3 that follows the ND is designed with $R_6 = 10 \text{ k}\Omega$ and variable R_7 ; R_7 is varied with a potentiometer to change the parameter b .

Figure 4: Nonlinearity of the Function

$$f(x_\tau) = -0.5n_1(|x_\tau| + x_\tau) + m_1 \tanh(l_1 x_\tau) : \quad \text{"n1"} \\ n_1 = 1.15, m_1 = 0.97, l_1 = 2.19; \quad \text{"n2"} \quad n_1 = 0.85, m_1 = 1, \\ l_1 = 4; \quad \text{"n3"} \quad n_1 = 0.5, m_1 = 1, l_1 = 5.$$

For the delay section, the APF is designed with the following parameters: $R = 10 \text{ k}\Omega$, $C = 10 \text{ nF}$, $R_8 = R_9 = 2.2 \text{ k}\Omega$. Each APF contributes a delay of $T_D \approx RC = 0.1 \text{ ms}$; thus the dimensionless parameter $\tau = \frac{RC}{R_0 C_0} = 1$, i.e., one needs i blocks to produce a delay $\tau = i$. In the experiment, we vary R to get variable delays. Note that one can also change R_0 to get a variable delay, but in that case the power spectral property of the circuit will be changed [15].

3.1 Variable b

We set the time delay at $T_D = 0.3 \text{ ms}$ (i.e., $\tau = 3$) by using three APF blocks each having $R = 10 \text{ k}\Omega$. To observe the behavior of the system for different b , we vary R_7 . For $R_7 \approx 9 \text{ k}\Omega$, the circuit shows a stable limit cycle of frequency 1000 Hz . At $R_7 = 16.1 \text{ k}\Omega$ (approx.), the limit cycle of period-1 loses its stability and a period-2 oscillation emerges. A period-4 behaviour is observed at $R_7 = 16.71 \text{ k}\Omega$ (approx.). Apparently, the circuit enters into the hyperchaotic region for $R_7 > 22 \text{ k}\Omega$. With further increase of R_7 , the circuit shows a large limit cycle at $R_7 \geq 23.5 \text{ k}\Omega$ that indicates the occurrence of boundary crises. All the above mentioned behaviours (except the large limit cycle) are shown in Figure 6 (in $V-V(t-T_D)$ space), depicting the real time oscilloscope traces.

Figure 5: Experimentally Obtained Nonlinearity Produced by the ND part of Figure 2.

3.2 Variable n

Now we set the time delay at $T_D = 0.4 \text{ ms}$ (i.e., $\tau = 4$) by using four APF blocks each having $R = 10 \text{ k}\Omega$ and $b \approx 1.1$ by keeping $R_7 = 11.08 \text{ k}\Omega$. We vary the system parameter n , by varying the resistance R_3 . For $R_3 \approx 6.90 \text{ k}\Omega$, the circuit shows a limit of period-1. Then at $R_3 \approx 3.35 \text{ k}\Omega$, the period-1 cycle converts to period-2 cycle. The circuit enters the chaotic regime at $R_3 \approx 2.62 \text{ k}\Omega$ (approx.). The hyperchaos emerges at $R_3 < 2.40 \text{ k}\Omega$ (approx.). The behavior of the circuit for different values of the above system parameter is shown in figure 7.

3.3 Variable m

Now the system is subjected to examine under the variation of the parameter m , viz., varying the resistance R_4 . For this the delay was kept at $\tau = 4$ and $b = 1.1$. At $R_4 = 17.58 \text{ k}\Omega$, the circuit emerges a limit cycle of period-1. Further at $R_4 = 14.51 \text{ k}\Omega$, the circuit is subjected to limit cycle of period-

2. Then at $R_4=13.02 \text{ k}\Omega$ (approx.), the circuit enters into the chaotic regime. Finally, the system emerges hyperchaos for $R_4=10.46 \text{ k}\Omega$ (approx.). The different situations of the aforesaid is shown in figure 8.

3.4 Variable l

The parameter l can be varied by varying the resistance R_1 . We keep the delay $\tau=4$ and $b=1.1$ for this purpose. At $R_1=14.39 \text{ k}\Omega$, the system emerges period-1 limit cycle. At $R_1=12.52 \text{ k}\Omega$, a limit cycle of period-2 is achieved. Then the system enters the chaotic regime at $R_1=11.40 \text{ k}\Omega$ (approx.). The hyperchaos is achieved for $R_1<11.06 \text{ k}\Omega$ (approx.). Figure 9 represents all these situations.

Figure 6: The Oscilloscope trace of Experimentally obtained phase-plane plots in the $V-V(t-T_D)$ space for variable R_7 : (a) period-1 at $R_7 = 12 \text{ k}\Omega$, (b) period-2 at $R_7 = 16.4 \text{ k}\Omega$, (c) period-4 at $R_7 = 16.72 \text{ k}\Omega$, (d) chaos at $R_7 = 16.9 \text{ k}\Omega$, (e) hyperchaos at $R_7 = 22.5 \text{ k}\Omega$, (f) hyperchaos at $R_7 = 23.3 \text{ k}\Omega$ (for other parameters see text). (a)–(e) V (x-axis): 0.5 v/div; $V(t-T_D)$ (y-axis): 0.5 v/div. (f) V (x-axis): 1 v/div; $V(t-T_D)$ (y-axis): 1 v/div.

Figure 7: The Oscilloscope trace of Experimentally obtained phase-plane plots in the $V-V(t-T_D)$ space for variable R_3 : (a) period-1 at $R_3 = 6.90 \text{ k}\Omega$, (b) period-2 at $R_3 = 3.35 \text{ k}\Omega$, (c) chaos at $R_3 = 2.62 \text{ k}\Omega$, (d) hyperchaos at $R_3 = 1.68 \text{ k}\Omega$. V (x-axis): 0.2 v/div; $V(t-T_D)$ (y-axis): 0.2 v/div.

Figure 8: The Oscilloscope trace of Experimentally obtained phase-plane plots in the $V-V(t-T_D)$ space for variable R_4 : (a) period-1 at $R_4 = 17.58 \text{ k}\Omega$, (b) period-2 at $R_4 = 14.51 \text{ k}\Omega$, (c) chaos at $R_4 = 13.02 \text{ k}\Omega$, (d) hyperchaos at $R_4 = 10.46 \text{ k}\Omega$. V (x-axis): 0.2 v/div; $V(t-T_D)$ (y-axis): 0.2 v/div.

Figure 9: The Oscilloscope trace of Experimentally obtained phase-plane plots in the $V-V(t-T_D)$ space for variable R_1 : (a) period-1 at $R_1 = 14.39 \text{ k}\Omega$, (b) period-2 at $R_1 = 12.52 \text{ k}\Omega$, (c) chaos at $R_1 = 11.35 \text{ k}\Omega$, (d) hyperchaos at $R_1 = 8.48 \text{ k}\Omega$. V (x-axis): 0.2 v/div; $V(t-T_D)$ (y-axis): 0.2 v/div.

IV. NUMERICAL STUDIES

We use the numerical method to corroborate the system over some limited system parameters. The system equation (4) is solved numerically using the fourth order Runge-Kutta algorithm with a step size $h=0.005$. We use a constant initial function $\phi(t)=1$ for $t \in [-\tau, 0]$. Intense care has been taken to allow the system to settle to the steady state by excluding the transients.

To explore the dynamics of the system we keep the delay fixed at $\tau=3$ and vary ' b '. It is observed that with increasing b , for $b<0.834=b_H$, the system shows a fixed point at $x=0$. For $b \geq b_H = 0.834$, the fixed point loses stability through Hopf bifurcation, and a stable limit cycle emerges. At $b=1.51$, the limit cycle of period-1(P1) becomes unstable and a period-2 (P2) cycle appears. Further period doubling occurs at $b=1.68$ (P2 to P4). Through period doubling bifurcations, the system enters into the chaotic regime at $b=1.73$. With further increase of b , at $b=2.1$, the system shows the emergence of hyperchaos. Finally the system equation shows diverging behavior beyond $b=2.52$, indicating boundary crises.

A phase plane representation in representative $x-x(t-\tau)$ plane for different b is shown in figure 10, which depicts: period-1 ($b=1.36$), period-2 ($b=1.64$), period-4 ($b=1.68$), chaos ($b=1.74$), hyperchaos ($b=2.1$ and 2.4). The plot of Lyapunov exponent (LE) verses b is shown in figure 11. Here

first ten LEs are plotted with b . From figure 11 it is clear that the system enters the chaotic regime at $b = 1.73$. For $b \geq 1.9$, two of the LEs become positive and finally at $b = 2.1$ the system becomes hyperchaotic one.

Figure 10: Phase Plane Plot in $x-x(t-\tau)$ space for Different b : (a) $b = 1.36$ (period-1), (b) $b = 1.64$ (period-2), (c) $b = 1.68$ (period-4), (d) $b = 1.74$ (chaos), (e) $b = 2.10$ (hyperchaos), (f) $b = 2.40$ (hyperchaos). Other parameters are: $\tau = 3$, $a = 1$, $n = 1.15$, $m = 0.97$, $l = 2.19$.

V. CONCLUSION

In this paper we have proposed the design of a new electronic circuit to realize the first order time-delay chaotic system. By the hardware experiment we see that, by varying the system parameter, say b , and keeping delay constant, the system

Figure 11: Lyapunov Exponent (λ) – b plot. First two LEs become positive for $b > 1.9$, indicating hyperchaos

shows chaotic and hyperchaotic behavior. A similar case arises when we keep system parameter b constant and vary the delay. We have also varied the parameters n , m , l respectively, and achieved the similar scenario. The numerical simulation of the system for some limited system parameters confirms our experimental results. Here we have identified that an active all pass filter could be used suitably to design a time delay block. For an APF, the power of the output signal does not attenuate at high frequency also. If we take a higher order APF, the time delay may be flat enough even for the higher frequencies. Thus, this new type of delay line may be useful for designing high frequency chaotic and hyperchaotic oscillators. We have shown that the experimental and the numerical results match well.

The proposed circuit is important from the practical application aspect in the way that with the suitable choice of the parameters, the system shows hyperchaotic behavior even for a small or moderate value of the time delay. So the system can be used as an efficient hyperchaotic generator for electronic communication application, chaos-based noise

generator system [14]. The present work creates a scope that one can systematically study the synchronization and control property of the system, which may be taken as a future work.

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