Techniques of Power Phase-Noise Optimization of 2.4 / 4.8 GHz CMOS VCO with Switched Capacitor Array Using Bondwire Inductor

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Abstract— This paper presents theoretical analysis of the maximum operating frequency of proposed Source Degeneration (SD) and Conventional CML D-Latch are estimated. The approach is based on the voltage transfer function, which is derived from small signal model of the circuit. Design approach with pre and post layout simulation results have been presented in detail and compared the performance in terms of power consumption, self oscillation frequency, sensitivity and supply voltage. With example shows the, all pMOS Voltage Controlled Oscillator (VCO) with MOS capacitor switched capacitor array (SCA) generates the high frequency sinewave reference signals fed in to both divider for to get quadrature (Q) sinewave signals. Off Chip Bondwire inductor is used instead of on chip spiral inductor in all-pMOS VCO as it have high quality factor. Also, it will neglect the variations of carrier frequency and it gives additional performance like phase noise, power consumption, area than using spiral inductor. Even if use spiral inductor in all-pMOS VCO, Bondwire inductor also presents due to low impedance path between drain and ground terminal. Various optimization techniques are implemented while designing a QVCO, which facilitates is used to achieve a low power low phase noise performance. Compared to other types of QVCO, the conventional QVCO shows good phase noise performance than normally achieved 6 dB phase noise improvement with carrier frequency. The simulated results shows about 5 dB, 4 dB, 4 dB and 4 dB of phase noise improvement at 10 kHz, 100 kHz, 1 MHz and 3 MHz offset frequency from the 2.4 GHz carrier frequen cy. This combinational topology doesn’t consume additional power and area than others and shows improved phase noise performance. The pre and post layout simulation results are compared of both proposed (SD) and conventional QVCO, which is designed in 180 nm CMOS technology as IV.

Keywords— VCO, CML Divider, Source Degeneration, Voltage Headroom, Supply Voltage, Bondwire Inductor

I. INTRODUCTION

D-LATCH is one of the basic functional blocks in Voltage Controlled Oscillator (VCO) and Phase Locked Loops applications for dividing upcoming frequency into specified frequency as connected in Master-Slave configuration. Apart from many types proposed so far [1], [2] Current Mode Logic (CML) D-Latch [3] is suitable for high frequency dividers due to low power consumption including occupies low area. Because, with tail current source has less voltage headroom whereas without tail current source has high voltage headroom in CML D Latch. Hence, it can capable to operate in low supply voltage operation due to additional overdrive voltage and gate source potential. In this paper, comparison of theoretical analysis of maximum operating frequency of proposed (SD) and conventional D-Latch are discussed. With example shows the further improvement changes in terms of area and cost of fabrication [2] replacing proposed SD-divider QVCO [4] into conventional divider QVCO without fixed tail current source. Also, changes in poly capacitor SCA [4] into MOS capacitor SCA further reduce in terms of cost of fabrication.

The paper is organized as follows. Section 2 describes about functional operation of proposed (SD) and conventional CML D-Latch. Section 3 describes about theoretical analysis of maximum operating frequency of proposed (SD) and conventional D-Latch. Section 4 discuss about circuit design at 4.8 GHz followed by comparison of pre and post layout simulation results. Section 5 discussed about all-pMOS VCO with MOS capacitor SCA including analysis of equivalent and phase noise model of VCO. Section 6 describes the various design techniques to achieve a low power low phase noise performance followed by simulation results and discussion in section 7.

II. WORKING PRINCIPLE OF PROPOSED (SD) AND CONVENTIONAL D-LATCH AND IT’S COMPARISONS

The proposed SD-CML Latch with resistive load [4] and CML latch with resistive load [2] are shown in Fig. 1 (a) and Fig. 1(b). The nMOS transistor M$_{1,2}$ act as pull down network is controlled by the differential data inputs ($V_a$ and $V_b$). The nMOS transistor M$_{2,6}$ act as pull down network is controlled by the differential data inputs ($V_a$ and $V_b$). It is used to push the dc current generated by reference voltage $V_{ref}$ and produce the differential outputs ($V_q$ and $V_{\bar{q}}$). The transistor M$_{3,4}$ operates in triode region, used for biasing the entire transistor. The transistor M$_{3,4}$ consists of cross coupled pair connected in positive feedback provides negative
transconductance to maximize the operating frequency. The load resistance ($R_{load}$), which can be implemented either poly resistors or active pMOS loads, whereas $R_s$ is source degeneration resistor. Source degeneration ($R_s$) (SD-CML) latch is used to reduce the harmonic distortion and close-in phase noise through linearization at the cost of lower gain. It also provides negative feedback, which acts to stabilize the bias current generated by $V_{ref1}$, resulting in predictable output swings. Due to high output resistance, it helps to reduce the current spikes occur at the drain terminal of the clocked transistors.

Now, let’s assume the latch operation after the arrival of the clock signal and data input [5]. When $V_{clk}$ is switching from logical ‘0’ to logical ‘1’ and $V_{clk}$ is switching from logical ‘1’ to logical ‘0’. The transistor $M_5$ is switched on, it will flows the entire current through differential pairs $M_1$ or $M_2$ based on the input data arrives. Consider the logic levels of the data inputs be $V_d = '1'$ and $V_d = '0'$, the transistor $M_1$ is turn on to push the entire current flows through transistors $M_3 - M_1$. The logic levels of the outputs after the arrival of the clock signal and data input is $V_q = '0'$ and $V_q = '1'$. Based on the input assumptions, the output capacitor at node $V_q$ will start discharging through transistors $M_4 - M_1$ and degeneration resistor ($R_s$), while the capacitor at node $V_{\bar{q}}$ is charging through load resistance ($R_{load}$).

A. Supply Voltage

The minimum supply voltage required for proposed SD-CML D-Latch is shown in Fig. 1 (a) as follows,

$$V_q = V_{DD} - I_d R_{load}$$  \hspace{1cm} (1)

Conditions for transistor ‘$M_1$’ operating in saturation region, Neglect body effect

$$V_q \geq V_d - V_{th1}$$  \hspace{1cm} (2)

The minimum input voltage at transistor ‘$M_1$’ is,

$$V_d (min) = V_{GS1} + I_d R_s + (V_{ds5} (linear \ region) \leq (V_{bias} + v_{clk} - V_{th5}))$$  \hspace{1cm} (3)

The maximum input voltage at transistor ‘$M_1$’ is,

$$V_d (max) = V_{DD} - I_d R_{load} + V_{th1}$$

Substitute (3) in (2),

$$V_q (min) = V_{GS1} + I_d R_s + V_{ds5} - V_{th1}$$  \hspace{1cm} (4)

Substitute (4) in (1),

$$V_{DD} \geq \frac{2I_d}{K} + I_d R_s + V_{ds5} + I_d R_{load}$$

Equation (5) is the minimum supply required for proposed SD-CML D-Latch.

Similarly,

$$V_{DD} \geq \frac{2I_d}{K} + V_{ds5} + I_d R_{load}$$

Equation (6) is the minimum supply voltage required for conventional CML D-Latch.

B. Theoretical Analysis of Maximum Operating Frequency Range

Proposed SD-CML Latch

The maximum operating frequency depends on how fast sensing operation is. The high frequency small signal half equivalent circuit shown in Fig. 1(a) is

$$V_q$$

Fig. 2. Small signal half Equivalent proposed SD-D-Latch

Where,

$C_t$ is total parasitic capacitance at node $V_q$, $R_{load}$ is negative input tansconductance of latch circuit.
Let us estimate the transfer function of D-latch by associating one pole with each node.

At node $V_q$ (Fig. 2), the sum of the currents is equal to zero,

Initially, some amount of charges is stored in total capacitance ($C_T$) due to presence of thermal noise ($KT/C_T$) to obtain self oscillation frequency ($f_{so}$) before applying any input to transistor $M_{1-5}$. After applying input when $V_d$ and $V_{Clk+}$ equal to ‘1’, total capacitance ($C_T$) starts to discharge through transistor $M_{1-5}$ and source degeneration resistor ($R_s$). Hence,

At node $V_q$,

$$G_m V_d' + \frac{V_q}{R_{load}} + \frac{V_d}{R_s} + \frac{1}{R_{out}} + s C_T V_q = 0$$

(7)

$$\frac{V_q}{V_d} = \frac{G_m}{R_s} - \frac{1}{R_{out}} - \frac{1}{R_{load}} - \frac{1}{R_s} - s C_T$$

(8)

Where, $G_m$ and $R_{out}$ is the effective transconductance and output resistance of transistor $M_1$,

$$G_m \approx \frac{g_m}{(1 + g_m R_s)}$$

$$R_{out} \approx r_{ds1} \left(1 + \left(g_m \cdot R_s\right)\right)$$

Equation (8) is the transfer function of proposed SD-CML D-Latch.

Now, let us calculate approximation value of maximum operating frequency when the voltage gain becomes unity. Neglect body effect and channel length modulation while considering in worst case analysis.

$$G_m + \frac{1}{R_{out}} + \frac{1}{R_{load}} + \frac{1}{R_s} + \frac{1}{g_m} + s C_T = 0$$

(9)

Replace’s’ is equal to j2nf in equation (3) to determine the operating frequency of proposed SD-CML D-Latch.

Equation (3) becomes,

$$\frac{V_q}{V_d} = \frac{G_m}{r_{ds1}} + \frac{1}{R_{load}} + \frac{1}{R_s} + s C_T$$

(10)

Squaring on both sides in equation (10),

$$f = \frac{-\left(g_m \cdot R_s\right)}{4 \Pi C_T}$$

(11)

Assume, $k = \frac{1}{R_s g_{m4} - 1}$

where,

$$R_s g_{m4} < 1$$

$$f = \frac{\left(-g_m^2 \cdot R_s\right)}{4 \Pi C_T^2} \left(\frac{1}{r_{ds1}} + \frac{1}{R_{load}} + \frac{1}{R_s} + \frac{1}{g_m}\right)^2$$

(12)

For maximum operating frequency, when $g_{m4}$ is equal to

$$\frac{1}{R_s} + \frac{1}{R_{load}}$$

Hence equation (12) becomes,

$$f_{max} = \frac{\left(G_m\right)}{2 \Pi C_T}$$

(13)

Equation (13) is the maximum operating frequency of proposed SD-D-Latch.

Conventional CML D-Latch

The small signal model of half equivalent CML D-Latch as shown in Fig. 3 is

At node $V_q$,

$$g_m V_d' + \frac{V_q}{R_{load}} - \frac{V_q}{R_{load}} + s C_T V_q = 0$$

(14)

$$\frac{V_q}{V_d} = \frac{1}{r_{ds1} + g_m - R_{load} - s C_T}$$

(15)

Equation (15) is the transfer function of conventional CML D-Latch.

Similarly, to find the maximum operating frequency of conventional CML D-Latch from equation (7) to equation (11) is,

$$f = \frac{-\left(g_m^2 \cdot R_s\right)}{4 \Pi C_T^2} \left(\frac{1}{r_{ds1}} + \frac{1}{R_{load}} + \frac{1}{R_s} + \frac{1}{g_m}\right)^2$$

(16)

Equation (16) is the operating frequency of conventional CML D-Latch.
Equation (17) is the maximum operating frequency of conventional CML D-Latch.

C. Comparison of Simulation Results

The input sensitivity of the divider is simulated the input range between 60 mV to 530 mV (p-p) to get high linearity signals without distortion. The input (p-p) voltage is greater than 530 mV (p-p), the signal gets distorted based on the design to meet the specifications. It can be seen that the proposed SD-CML divider has a bandwidth of 3.2 to 6.2 GHz as a self-oscillation frequency of fso is equal to 4.6 GHz shown in Fig. 4. At this frequency the divider gets self oscillates with floating driving inputs. Similarly, in conventional CML Divider also achieve a bandwidth of 3.0 to 6.4 GHz with same power consumption and supply voltage with respect to input voltage ranges between 50 mV to 550 mV is shown in Fig. 5.

![Fig. 4. Sensitivity of Proposed SD-CML Divider](image1)

![Fig. 5. Sensitivity of conventional Divider](image2)

The maximum operating frequency of both dividers is derived as shown in equation (13) and (17) and determined at which device size gives maximum operating frequency shown in Fig. 6.

The comparison of pre and post layout results in terms of self oscillation frequency, power consumption and sensitivity of proposed and conventional divider is shown in Table 1. Fig. 7 (a) and (b) are layout of proposed SD- and conventional CML D-Latch.

<table>
<thead>
<tr>
<th>Temperature (−40 ~ 85 °C)</th>
<th>Self Oscillation Frequency (fso) (GHz)</th>
<th>Sensitivity (mV)</th>
<th>Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre Layout (Proposed)</td>
<td>3.2 ~ 2.0</td>
<td>60 ~ 530</td>
<td>1.6 ~ 1.2</td>
</tr>
<tr>
<td>Post Layout (Proposed)</td>
<td>2.4 ~ 1.8</td>
<td>150 ~ 600</td>
<td>1.6 ~ 1.2</td>
</tr>
<tr>
<td>Pre Layout (Conventional)</td>
<td>4.3 ~ 3.1</td>
<td>50 ~ 550</td>
<td>1.6 ~ 1.2</td>
</tr>
<tr>
<td>Post Layout (Conventional)</td>
<td>2.3 ~ 1.7</td>
<td>100 ~ 600</td>
<td>1.6 ~ 1.2</td>
</tr>
</tbody>
</table>

![Fig. 4. Sensitivity of Proposed SD-CML Divider](image3)

![Fig. 5. Sensitivity of conventional Divider](image4)

![Fig. 6. Maximum Operating Frequency vs. Device Size Ratio](image5)

![Fig. 7. Layout of Divider for Generation of Quadrature Signals](image6)

![Fig. 7. Layout of Divider for Generation of Quadrature Signals](image7)

III. DESIGN OF VCO WITH MOS CAPACITOR SCA

The high linearity reference clock signals shown in Fig. 8 generating by combination of inductor, capacitor (LC) oscillator to get required tuning range say 2.4 – 2.5 GHz. To meet the specified tuning range, VCO needs to generate 4.8 – 5 GHz by varying the MOS capacitance called MOS varactor with the help of applying voltage called voltage controlled oscillator (VCO). The performance comparison of three types of VCO in terms of supply voltage, tuning range and varactor noise is discussed [6]. The performance comparison of VCO using various loads either active or passive tuned by different varactors are discussed [7] in terms of close in phase noise, harmonic distortion, frequency range and amplitude swing (p-p). The overall performance is displayed by active load using MOS transistor and I-pMOS varactor. Schematic of all-pMOS LC-VCO with MOS capacitor SCA is shown in Fig. 8. The
all-pMOS LC-VCO is designed in 0.18 µm CMOS technology and the supply voltage is 1 V. M1 and M2 form a pMOS current mirror, whereas M3 and M4 are coupled in a positive feedback to provide negative resistance in order to compensate the losses occur due to parasitic resistance of both inductor and capacitor. M5 and M6 are inversion-mode pMOS (I-pMOS) varactor, which is used to vary the capacitance whose value is dependent on the control voltage (V_{ctrl}). The bias current (I_{bias}) is generated by V_{ref}. 4 bit binary weighted MOS capacitor SCA is used, which is best suited for low cost applications as it occupies small area than poly capacitor SCA [1]. It is used for coarse tuning by discrete switches (D0, D1, D2, D3) while maintaining a constant VCO tuning gain (K_{VCO}) at low supply voltage. An advantage of all-pMOS LC-VCO compared with other topologies [4] is power supply (V_{DD}) noise isolated through pMOS bias circuit to V_{DD} and ground referenced tank [8]. Before going in to actual design, find the six parameters value of on-chip spiral inductor either using MATLAB from given S-parameters [6] or using ASITIC or by standardized quality factor of on-chip spiral inductor (1 ~ 10 nH) around 5 ~ 10. By assumption, the value of each inductor is 1 nH. The parasitic resistance of the spiral inductor was found approximately 4.5 ohm providing a (Q) value of 6.7 at 4.8 GHz estimated using ASITIC [9].

Fig. 8: Schematic of all-pMOS LC-VCO with MOS Capacitor SCA

D. Equivalent and Phase Noise model of LC-VCO With MOS Capacitor SCA

The equivalent and phase noise model of LC-VCO with MOS capacitor SCA as shown in Fig. 9 (a) and 9 (b).

Fig. 9 (a). Equivalent Small Signal Model of LC VCO with MOS Capacitor SCA
When the MOS SCA switches is on,

\[ R_T = R_{PS} \parallel R_{PV} \parallel R_{P1} \]

\[ C_T = C_{PV} + C_{PSCA} + C_{load} + C_{P1} + C_{pMOS} \]

When the MOS SCA is off,

\[ R_T = R_{PS} \parallel R_{PV} \parallel R_{P1} \]

\[ C_T = C_{PV} + C_{equ} + C_{load} + C_{P1} + C_{pMOS} \]

\[ R_{P1} \text{ and } C_{P1} \text{ are the substrate parasitic resistance and } \text{capacitance to ground. } R_{PS} \text{ and } R_{PV} \text{ are the parallel inductance and MOS varactor resistance.} \]

\[ g_{m3} = \frac{1}{R_T} \]

IV. DESIGN OF QUADRATURE SIGNALS

The divider used for generate quadrature (Q) sinewave reference signals, is combination of two D-Latch shown in Fig. 1(a) and 1(b) connected in master-slave configuration. The block diagram of divider used for generating quadrature signals is shown in Fig. 10.

The design is completely designed in 0.18 \( \mu \)m CMOS process technology as the supply voltage is ‘1’ V instead of 1.8 V by equation (5) and (6). The current drawn from supply voltage is each D-Latch is approx. 700 \( \mu \)A. Total power consumption of divider is approx. 1.4 mW at ‘1’ V supply voltage.

V. VARIOUS DESIGN TECHNIQUES TO ACHIEVE A LOW POWER LOW PHASE NOISE QVCO

The various design techniques is implemented while designing a low power low phase noise QVCO for wireless applications as follows,

a. Major contributions of flicker noise (1/f) are mostly dependent on current source (M2) than switching transistor (M3 and M4) (Fig. 1). PMOS based current source have approximately ~10 dB lower 1/f noise compared to that for nMOS based current source. This is because pMOS have buried channel whereas nMOS have surface channel. For additional suppression of 1/f noise, increase the length and width of the bias transistor (M2) [8]. The phase noise performance of bias transistor is also affected by common mode node variations (\( v_{cm} \)). This issue can be solved by increasing the output resistance of bias transistor to make less variation in fixed bias current. For this, choose the channel length of bias transistor is usually about 4-5 times of \( L_{min} \).

b. Noise comes from reference circuit (\( V_{ref} \)) coupled with M1 then amplified with M2 (Fig. 1), which degrade the phase noise performance of whole QVCO. To overcome these problems, insert the high value of on-chip resistor (R) and high value of on-chip capacitor (C) between M1 and M2 to form as low pass filter. Flicker and thermal noise from the reference circuit are rejected at frequencies above the filter corner frequencies [8].

c. Switching transistor (M3 and M4) in all-pMOS VCO contribute \( 1/f \) noise, which is mostly dependent on overdrive voltage (\( V_{gs} - V_{th} \)) [11]. To increase the overdrive voltage with fixed bias current by vary the device size (\( W_p \)) of transistors. This helps to further
reduce the 1/f bias noise by increasing the $V_{gs} - V_t$. Also, the switching transistors contribute 1/f noise, which is reducing by increasing the overdrive voltage. This tends to further reduce the higher order harmonic signals like 3rd due to linearity of transistor but some limit by varying the device size. Proper size required for transistors to obtain a large transconductance value to ensure proper startup of the VCO but sufficiently small to reduce the thermal noise.

d. The bias transistor (M2) operated in either current or voltage limited regime, which helps to reduce the both power and phase noise performance. In current-limited mode of operation, the tank amplitude increases proportionally with tail current ($I_{bias}$) and tank equivalent resistance ($R_T$) until oscillator reaches the voltage limited regime [12]. In voltage limited mode of operation, amplitude limited by supply voltage ($V_{DD}$). Hence, further increasing $I_{bias}$, where the oscillator meets between those regimes, is fully wastage of power and it affects the phase noise performance. The phase noise relationship with tail current to identify the current and voltage limited regime [12]. From that definition it will choose the proper bias current which is used to reduce the both power and phase noise performance.

e. Switched Capacitor Array (SCA) is used to increase the overall quality factor ($Q$) of total capacitor ($C_T$) which includes parallel combination of equivalent MOS varactor and SCA capacitor (Fig. 1). ‘$Q$’ is limited by the finite turn-on resistance ($R_{SCA}$) of MOS transistor. To reduce the $R_{SCA}$, the device width of nMOS switches is made larger, while keeping the minimum channel length ($L_{min}$). At the same moment it will raise the parasitic capacitance of MOS transistor which will limit the tuning range of VCO. Hence, there is a tradeoff between tuning range and quality factor. Proper device size of switches is needed to achieve both quality factor and tuning range specified in targeted specifications.

f. Another approach used to reduce the 1/f noise is the increase of transistor area (WL). If WL is increased while keeping W/L ratio constant then the device transconductance and thermal noise remained same but the device capacitance will increase [13]. Hence, there is a tradeoff between self oscillation frequency and 1/f noise of the divider. Usually selects a channel length (L) of about 25% to 50% greater than $L_{min}$ [14]. This approach has been implemented while designing a conventional as well as proposed divider.

g. Practical passive devices like poly-resistor, capacitor also contribute 1/f noise. To reduce the 1/f noise, increase the width of resistor or reduce the voltage drop across the resistors [10]. At the same instance it will raise the parasitic capacitance, which limits the maximum operating frequency.

h. As the input signal amplitude of divider is very large, the transistor operates close to 1 dB compression point [1] thereby, nonlinearity of the device is directly coupled to phase noise characteristics. Hence, the minimum and maximum required value of input amplitude of divider can be found by the sensitivity of the divider [15]. These values should satisfy various operating conditions like temperature variations, process corner analysis and inaccurate inductor modeling. If the input amplitude exceeds those ranges, output may get distorted and it will contribute 1/f noise.

i. By Friis formula [16], if design has multiple blocks like cascading structure the gain of first stage is higher than second stage, whereas second stage is higher than third but lower than first stage based on ‘N’ stage. It is useful to reduce and bring down the noise factor approximately equal to one. In this design, VCO followed by divider then followed by buffer is used.

j. The reference voltage of divider without fixed tail current source also affects close in phase noise due to tail transistor operating in linear mode region. For that reason, by trial and error method with consideration of voltage headroom choose appropriate reference voltage.

VI. LAYOUT DESIGN AND IT’S RESULTS

The proposed (SD) and conventional D-Latch without fixed tail current source QVCO has been designed and compared the performance using different varactors in terms of phase noise, phase error and power consumption implemented in 0.18 μm standard CMOS technology [17][7]. The overall performance is displayed by inversion mode pMOS varactor. Bandgap reference is used to generate the reference voltage for all the sub blocks like VCO followed by divider then followed by buffer, which is independent of temperature and supply independent. The comparison of pre and post layout simulation results is described as follows.

### Table III: Simulation Results of Proposed SD-QVCO with Different Process Corners

<table>
<thead>
<tr>
<th>Temperature (−40 °C ~ 85 °C)</th>
<th>Layout</th>
<th>FF</th>
<th>TT</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuning Range (GHz)</td>
<td>Pre</td>
<td>2.49 ~ 2.38</td>
<td>2.50 ~ 2.39</td>
<td>2.46 ~ 2.39</td>
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<tr>
<td></td>
<td>Post</td>
<td>2.21 ~ 2.10</td>
<td>2.22 ~ 2.11</td>
<td>2.18 ~ 2.11</td>
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<tr>
<td></td>
<td></td>
<td>−127 ~ −126</td>
<td>−127 ~ −126</td>
<td>−118 ~ −125</td>
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<tr>
<td>Phase Noise @1 MHz dBc/Hz</td>
<td>Pre</td>
<td>−120 ~ −122</td>
<td>−121 ~ −124</td>
<td>−119 ~ −121</td>
</tr>
<tr>
<td></td>
<td>Post</td>
<td>5.1 ~ 4.9</td>
<td>4.6 ~ 4.7</td>
<td>4.2 ~ 4.3</td>
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<td></td>
<td></td>
<td>6.859 ~ 6.7</td>
<td>5.535 ~ 5.54</td>
<td>4.1 ~ 4.5</td>
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<td>Power Dissipation (mW)</td>
<td>Pre</td>
<td>−38 ~ −32</td>
<td>−44 ~ −39</td>
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<td></td>
<td>Post</td>
<td>−38 ~ −32</td>
<td>−44 ~ −39</td>
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<td>Harm. Distortion (3rd) (dBC)</td>
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<td>−3.18 ~ 2.33</td>
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<tr>
<td></td>
<td>Post</td>
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<td>2.233 ~ 1.798</td>
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<td>Self Osc. freq.of divider (GHz)</td>
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<td>3 ~ 2.165</td>
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Table III: Simulation Results of Conventional QVCO with Different Process Corners

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<th>Temperature (−40 °C ~ 85 °C)</th>
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<th>TT</th>
<th>SS</th>
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<tr>
<td>Tuning Range (GHz)</td>
<td>Pre</td>
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<td>2.51 ~ 2.38</td>
<td>2.50 ~ 2.38</td>
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<tr>
<td></td>
<td>Post</td>
<td>2.29 ~ 2.16</td>
<td>2.31 ~ 2.18</td>
<td>2.30 ~ 2.18</td>
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<tr>
<td>Phase Noise @3 MHz dBc/Hz</td>
<td>Pre</td>
<td>−136 ~ −134</td>
<td>−136 ~ −133</td>
<td>−135 ~ −132</td>
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<tr>
<td></td>
<td>Post</td>
<td>−124 ~ −126</td>
<td>−125 ~ −128</td>
<td>−123 ~ −125</td>
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<td>Power Dissipation (mW)</td>
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<td>Post</td>
<td>6.30 ~ 5.59</td>
<td>5.08 ~ 5.09</td>
<td>4.05 ~ 3.36</td>
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<td>Harm. Distortion (3rd) (dBc)</td>
<td>Pre</td>
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<td>−33 ~ −30</td>
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</tr>
<tr>
<td></td>
<td>Post</td>
<td>−24 ~ −29</td>
<td>−28 ~ −38</td>
<td>−33 ~ −42</td>
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<tr>
<td>Self Osc. freq.of divider (GHz)</td>
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<td>4.04 ~ 3.28</td>
<td>3.83 ~ 3.08</td>
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<td></td>
<td>Post</td>
<td>2.27 ~ 1.87</td>
<td>2.17 ~ 1.76</td>
<td>2.08 ~ 1.65</td>
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<td>Reference Voltage (mV)</td>
<td>Pre</td>
<td>553 ~ 530</td>
<td>551 ~ 527</td>
<td>550 ~ 524</td>
</tr>
<tr>
<td></td>
<td>Post</td>
<td>552 ~ 535</td>
<td>551 ~ 531</td>
<td>549 ~ 529</td>
</tr>
</tbody>
</table>

The pre and post layout simulation results of proposed SD-QVCO without bandgap reference are compared the performance in terms of tuning range, phase noise, power dissipation, harmonic distortion, and self oscillation frequency of divider, are analyzed over temperature and process corner variation is shown in table II. With consideration of bandgap reference, conventional QVCO are shown in table III. Due to lack of author’s laboratory, instead of on-chip spiral inductor, bondwire inductor is used while doing the layout design connected as external with assigning the quality factor of ‘8’s’ shown in Fig. 14. There is a possibility of threshold voltage variations by discarding wafers that fall out of the envelope [1]. Based on those reason the carrier frequency shifts by gate delay of the transistor. By using SCA will bring back to the carrier frequency. Drawbacks of proposed source degeneration in terms of area, mismatch, noise floor frequency and cost of fabrication [13]. To overcome the drawbacks, conventional QVCO are used with same performance achieved by using various optimization techniques discussed in section V. Hence, further will discuss about only conventional QVCO than proposed QVCO without fixed tail current source. The simulated results of conventional QVCO can be tuned from 2.38 to 2.51 GHz when all the discrete switches of SCA are 4’b1000. The overall performance of phase noise shows −133.6 dBc / Hz at 3 MHz offset from the carrier frequency, while consuming 5.17 mA of total current. The in-phase and quadrature signals simulated at 2.4 / 4.8 GHz conventional QVCO are depicted in Fig. 11. It can be figured out that the phase error between the two signals is 1.2° than 3° [4].

(a)VCO at 4.8 GHz. (b) Divider at 2.4 GHz. (c) Buffer

Figure 11. Differential Output Sinewave Signals

Fig. 12 shows the simulated phase noise of conventional QVCO than proposed SD-QVCO [4] using pMOS tail source at 4.8 GHz is −67 dBc, −94 dBc, −116 dBc, −125 dBc at 10 kHz, 100 kHz, 1 MHz and 3 MHz offset frequencies. Similarly, the simulated phase noise performance of combined QVCO at 2.4 GHz is plotted in Fig. 8. The phase noise at 2.4 GHz carrier frequency is −78 dBc, −104 dBc, −126 dBc and −135 dBc at 10 kHz, 100 kHz, 1 MHz and 3 MHz offset frequencies. In general, there is an additional 6 dB phase noise reduction will achieve this topology than any other QVCO’s like double cross coupled complementary QVCO with similar area constraints. For example, the value of on-chip spiral inductor used is 1 nH. Inductor parasitic has been estimated using ASITIC simulation results. The loss resistance value was found to be approximately 4.5 ohm providing a Q value of 6.7 as compared to a Q of 3.35 at 2.4 GHz with similar area constraints. Due to doubling ‘Q’ value, the phase noise reduces 6 dB (19). By (19), further phase noise improvement can be achieved for a QVCO is shown about 5.0 dB, 4.0 dB, 4.0 dB and 4 dB at 10 kHz, 100 kHz, 1 MHz and 3 MHz offset from the carrier frequency, respectively.
Monte Carlo statistical simulations have been undertaken over the QVCO extracted view shown in Fig. 13. The number of samples 'N' is 500. During simulations, component mismatches are considered. The scale X-axis is replace into frequency (GHz), whereas Y-axis is replace into number of samples.

VII. CONCLUSION AND FUTURE WORK

Several techniques has been presented to achieve a low power low phase noise 2.4 / 4.8 GHz CMOS VCO implemented in 1 V supply. Also, comparison of proposed and conventional CML divider has been presented and results are analyzed both pre and post layout. Implement the QVCO (or) VCO design from low to high multi-band or single band say at 2.4 GHz carrier frequency for short range wireless applications and tape-out the IC in less than 180 nm (scaling down the channel length upto 45 nm) standard CMOS technology and compare the results also, in BiCMOS technology. Also, changes in design configuration say in all-pMOS QVCO like MEMS Varactor, Spiral Inductor, active inductor, MEMS Inductor and only pMOS device (resistive load) with and without CML D-latch and compare pre and post layout simulation with fabricated results. Also, to achieve a low power, operational amplifier is used to integrate with high frequency VCO. For QVCO, double cross coupling VCO, Ring VCO and single cross coupling VCO with various divider types implement in standard digital CMOS (scaling down the channel length upto 45 nm), BiCMOS technology and compare the results with fabricated results. Also, six parameter values of on-chip spiral inductor obtained using MATLAB and import those values obtained from S-parameters using MATLAB in circuit simulator like CADENCE, Agilent ADS, and Electromagnetic simulator like ASITIC, IE3D and compare the results.

REFERENCES

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