Design and Development of Gaussian Minimum Shift Keying (GMSK) Demodulator for Satellite Communication

Pradeep Kumar Govindaiah

Abstract--- *This paper discusses DSP based implementation of Gaussian Minimum Shift Keying (GMSK) demodulator using Polarity type Costas loop. The demodulator consists of a Polarity type Costas loop for carrier recovery, data recovery, and phase detection. Carrier has been recovered using a loop of center-frequency locking scheme as in M-ary Phase Shift Keying (MPSK) Polarity type Costas-loop. Phase unwrapping and Bit-Reconstruction is presented in detail. All the modules are first modeled in MATLAB (Simulink) and Systemview. After bit true simulation, the design is coded in VHDL and code simulation is done using QuestaSim 6.3c. The design is targeted to Virtex-4 XC4VSX35-10FF668 Xilinx FPGA (Field programmable gate array) for real time testing, which is carried out on Xtreme DSP development platform.*

Keywords--- *Nyquist Filter, Bandwidth-Time Product, Inter-Symbol-Interference (ISI), Phase Wrapping, Phase Unwrapping*

I. INTRODUCTION

A Major requirement of satellite communication system is to reduce the amount of required transmission power and bandwidth. As the available resource is power and bandwidth, often a trade-off is made between the power and bandwidth based on a particular application. Gaussian Minimum Shift Keying (GMSK) provides the best performance in terms of the required bandwidth and the required power for the transmission.

After several years of research effort, the Consultative Committee for Space Data Systems (CCSDS) has mandated the exclusive use of GMSK with bandwidth-time product BTb = 0.5 for all interplanetary missions with transmitted bit rates higher than 2 Mbps. For near-Earth missions, instead, GMSK with BTb = 0.25 is one of the recommended CCSDS options, thereby potentially allowing for the same demodulator for interplanetary and non- interplanetary missions[1].

Gaussian Minimum Shift Keying (GMSK) has been the most common modulation format belonging to the class of partial response Continuous Phase Modulation (CPM) scheme. It is primarily adopted in the GSM standards for land mobile radio communication systems with BT_b = 0.3 because of its high bandwidth efficiency and constant envelope modulation characteristics which reduces the required power.

II. MATHEMATICAL ASPECTS OF GMSK MODULATOR AND DEMODULATOR

A. GMSK Modulator

GMSK is "Gaussian filtered MSK" is a form of continuous phase modulation, in which the input bits with, rectangular (+1, -1) shaping is converted to Gaussian pulses by a Gaussian low-pass filter which is a non-Nyquist filter before further modulation by a frequency modulator.

Due to the use of a non-Nyquist Gaussian filter the input pulses overlap, giving rise to a phenomenon known as Inter-Symbol Interference (ISI). The extent of this overlap is determined by the product of the bandwidth of the Gaussian filter and the data-bit duration (BT product). Due to ISI the spectrum becomes compact thus, increasing bandwidth efficiency. Even though we may have to supply an additional power by an amount of 6 dB to counter ISI at the demodulator it meets the requirements of ACI (the GMSK spectrum has the first side lobe which gives an attenuation of 40-60 dB) and gives a compact spectrum due to the introduction of ISI so that more channels can be placed in the available bandwidth.

One of the efficient algorithms for the implementation of GMSK Modulator is the Quadrature modulator structure. This structure consists of two major blocks, a quadrature base-band processor followed by I/Q Modulator. The modulation index can be exactly maintained at m=0.5 with this method[2]. The block diagram of Quadrature modulator structure is as shown in figure 1.

The GMSK Signal generated using the above Quadrature Structure is given by

$$s(t) = I(t)\cos(2\pi f_c t) + Q(t)\sin(2\pi f_c t) \qquad (1)$$

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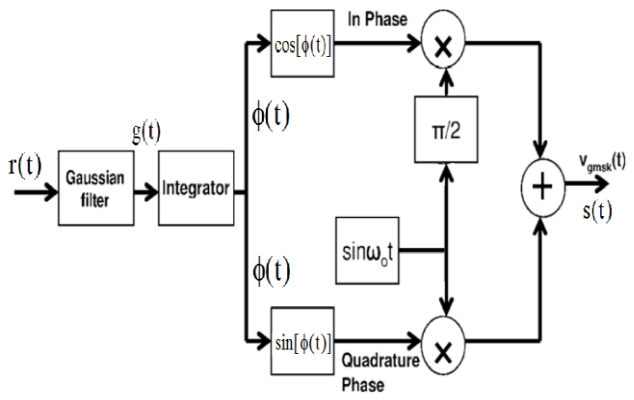

Figure 1: GMSK Modulator (Quadrature Structure)

B. GMSK Demodulator

A variety of different types of receivers exist for coherent detection of GMSK signal. The demodulator can be implemented in different optimum and sub-optimum methods.

In this paper demodulation of GMSK signal is carried out considering as a partial response continuous phase modulation signal[6].

If the GMSK signal is considered as a partial response continuous phase modulation signal (with modulation index of 1/2), then the receiver is made of an ideal multiplier that multiplies the received signal with a locally generated carrier, followed by low-pass filters to generate the real and imaginary parts of the complex envelope of the received signal. Then a phase generator builds all the possible phase transitions, finally the bits are reconstructed.

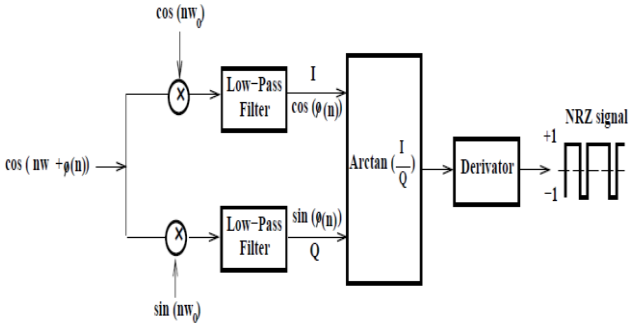

Figure 2: Block Diagram of I & Q Implementation of GMSK Demodulation

The Costas loop performs both phase-coherent suppressed carrier reconstruction and synchronous data detection within the loop. The upper loop is referred to as the quadrature, or tracking loop, and functions as a typical PLL, providing a data-corrupted error signal, $Z_c(t)$. The lower in-phase, or decision loop provides data extraction at the output of the lower mixer, and corrects the data corruption of $Z_c(t)$. The corrected error signal, $Z_o(t)$, is applied through loop filter F(s) to the VCO, which yields a phase estimate and generate the carrier signal[11].

A modified (hard-limited) Costas loop used for the demodulation of GMSK signals is shown in Figure 3.

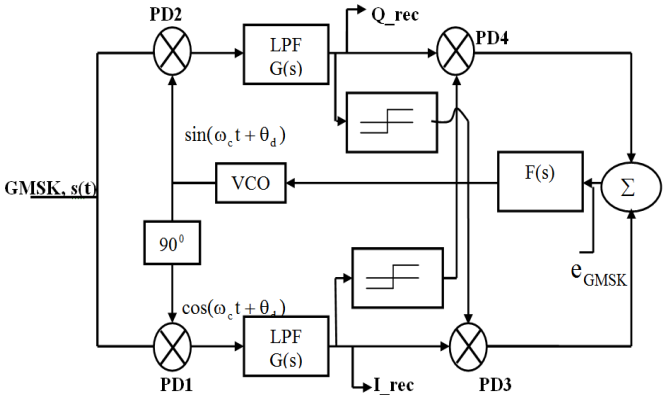

Figure 3: Polarity Type Costas Loop for Carrier Recovery

From equation (1) we have the GMSK signal using I-Q modulation methods,

$$s(t) = I(t)\cos(2\pi f_c t) + Q(t)\sin(2\pi f_c t), \quad (2)$$

The received signal under ideal conditions, can be given as,

$$s(t) = I(t)\cos(2\pi f_c t + \theta_d(t)) + Q(t)\sin(2\pi f_c t + \theta_d(t)) \quad (3)$$

where, $\theta_d(t)$ is the frequency deviation occurred due to channel characteristics.

The output of PD1 is given as

$$\cos(2\pi f_c t + \theta_o(t) * s(t) \quad (4)$$

where $\theta_o(t)$ is the initial offset in the VCO of the carrier recovery loop.

$$= \cos(2\pi f_c t + \theta_o(t)) * [I(t)\cos(2\pi f_c t + \theta_d(t)) + Q(t)\sin(2\pi f_c t + \theta_d(t))] \quad (5)$$

$$= \frac{I(t)}{2}[\cos(4\pi f_c t + \theta_o(t) + \theta_d(t)) + \cos(\theta_o(t) - \theta_d(t))] +$$

$$+ \frac{Q(t)}{2}[\sin(4\pi f_c t + \theta_o(t) + \theta_d(t)) - \sin(\theta_o(t) - \theta_d(t))] \quad (6)$$

The output of PD2 is given by

$$\sin(2\pi f_c t + \theta_o(t) * s(t) \quad (7)$$

$$= \sin(2\pi f_c t + \theta_o(t)) * [I(t)\cos(2\pi f_c t + \theta_d(t)) + Q(t)\sin(2\pi f_c t + \theta_d(t))] \quad (8)$$

$$= \frac{I(t)}{2}[\sin(4\pi f_c t + \theta_o(t) + \theta_d(t)) + \sin(\theta_o(t) - \theta_d(t))]$$

$$-\frac{Q(t)}{2}[\cos(4\pi f_c t+\theta_o(t)+\theta_d(t))-\cos(\theta_o(t)-\theta_d(t))] \quad (9)$$

Passing signals of equation (9) the I-arm and Q-arm becomes

I-arm component,

$$i(t)=\frac{I(t)}{2}[\cos(\theta_o(t)-\theta_d(t))]-\frac{Q(t)}{2}[\sin(\theta_o(t)-\theta_d(t))] \quad (10)$$

Q-arm component,

$$q(t)=\frac{I(t)}{2}[\sin(\theta_o(t)-\theta_d(t))]+\frac{Q(t)}{2}[\cos(\theta_o(t)-\theta_d(t))] \quad (11)$$

the error signal applied through loop filter F(s) to VCO is given by

$$e_{GMSK}=\{\text{sgn}[i(t)]*q(t)-\text{sgn}[q(t)]*i(t)\} \quad (12)$$

I_rec and Q_rec components are obtained at the output of the Low-pass filters of I-arm and Q-arm respectively as shown in the figure 3, the phase information is obtained by arctan operation. The phase information obtained is wrapped phase information, which has to be unwrapped before performing the differentiation. The wrapped phase information lies between + π to $-\pi$.

III. Related Work Section: Unwrapping the Phase Obtained from ARC Tan Operation

Unwrapping of the phase obtained is performed by the following steps given below and as shown in figure 4.

Step 1. Differentiating the wrapped phase which gives the glitches extended to both positive and negative sides of the data obtained.

Step 2. Detection of the positive and negative glitches is done.

Step 3. Set and reset circuit to generate the control signal to the up down counter.

Step 4. Positive glitches detection is given to the set circuit and negative glitches detection is given to the Reset circuit as shown in the figure 5.

Step 5. Output of the Set and Reset circuit is given to control input of the up down counter which generates the multiples of 2*pi which is to be added to wrapped phase to obtain the unwrapped phase.

Step 6. Finally the unwrapped phase is differentiated to recover the data.

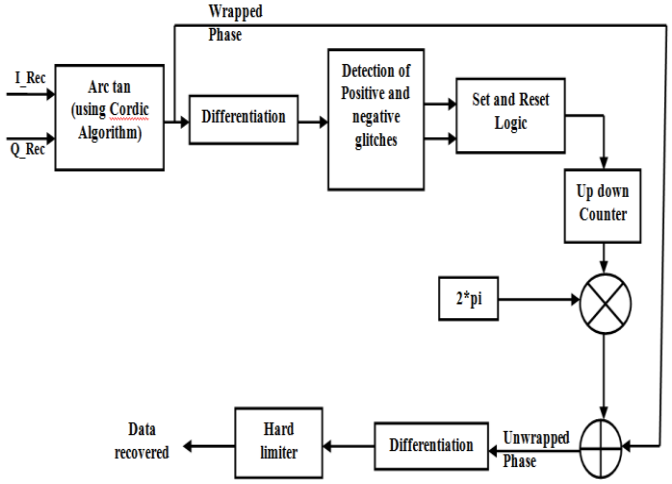

Figure 4: Phase Unwrapping and Bit Reconstruction

The set and reset Logic is as given in figure 5.

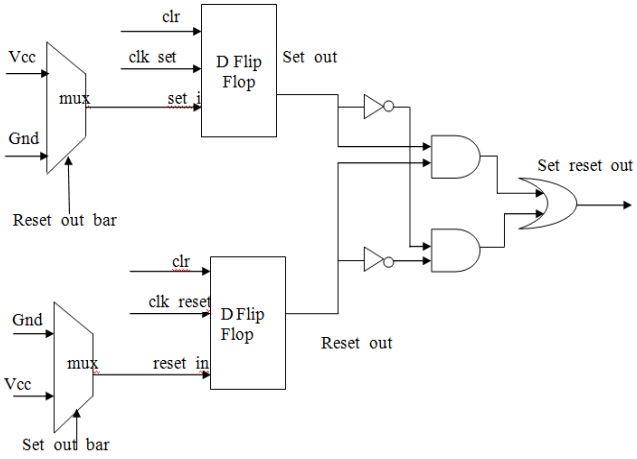

Figure 5: Set and Reset Logic

IV. In-Phase / Mid-Phase Synchronizer (for Clock Recovery)

This bit synchronizer also refers as Data transition tracking loop (DTTL)[4]. It operates in a closed loop and combines the operations of bit detection and bit synchronization. The In phase / Mid Phase synchronizer is employed at low SNR and medium data rates. It also operates well even in the presence of relatively long one's and zero's.

The In phase branch determines the polarity of the bit transition, when and if they occur, while the mid phase channel determines the magnitude of the bit-timing error. Use of both channels in the multiplier provides the correct sign of the timing error. The filtered output of the multiplier is used to drive the Numerically Controlled Oscillator (NCO) and timing circuit is designed to control the integrate-and-dump operations as shown in figure 6. It is possible to improve noise performance while SNR is above threshold by narrowing the mid phase integration window to T/4[4].

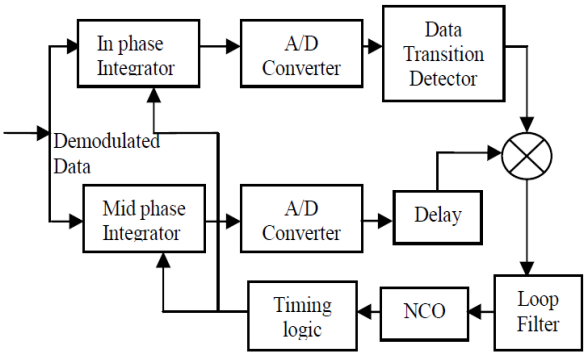

Figure 6: Inphase and Midphase Synchronizer (DTTL)

The bit synchronizer can be modeled as a PLL with feedback system as shown in figure 7. Given the requirement of bit synchronizer in terms of natural frequency ω_n and damping factor ξ, system can be modeled in terms of K_{pd}, Kvco, K1 and K2 which are defined below. The close loop transfer function of above loop is given by.

$$CLTF(s) = \frac{K_{pd}K_{VCO}\frac{F(s)}{S}}{1 + K_{pd}K_{VCO}\frac{F(s)}{S}} \quad (13)$$

where,

K_{pd} = Phase detector gain in Volts/radian

K_{VCO} = Sensitivity of VCO in rad/sec/volts

$F(s)$ = Loop filter transfer function

$$K = K_{pd}K_{VCO} \quad (14)$$

The equation (13) can be written as,

$$CLTF(s) = \frac{K\frac{F(s)}{S}}{1 + K\frac{F(s)}{S}} = \frac{KF(s)}{S + KF(s)} \quad (15)$$

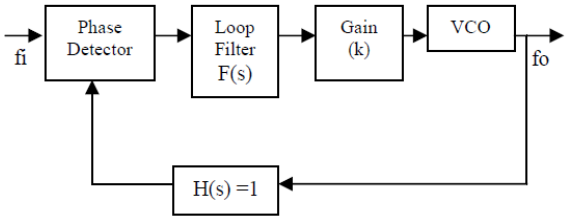

Figure 7: Phase Locked Loop

Depending on the choice of F(s), the CLTF(s) can be either first or second order system. For example, for type-2 systems, loop filter structure is shown in figure 8. Where,

$$F(s) = K1 + \frac{K2}{s}, \quad (16)$$

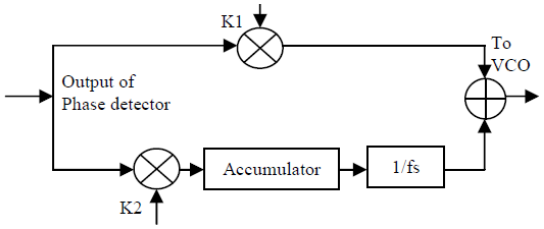

Figure 8: Loop Filter

Substituting equation (16) in equation (15), becomes

$$CLTF(s) = \frac{K * K1s + K * K2}{s^2 + K * K1s + K * K2} \quad (17)$$

which is of type 2, 2nd order system. Using servo theory, equation (17) is of the form

$$= \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (18)$$

Where,

$$K = K_{pd}K_{VCO} \quad (19)$$

The value of K_{pd} and K_{VCO} depends on f_S and the magnitude of the accumulator.

The value of K1 and K2 can be calculated by

$$\omega_n = \sqrt{K_{pd}K_{VCO}K2} \quad (20)$$

$$\xi = \frac{K_{pd}K_{VCO}K1}{2\omega_n} \quad (21)$$

The equations (13) to (21) are sufficient to model the bit synchronizer, and by changing the value of K1 and K2 we can control the performance and characteristics of demodulator loop. The stability of the system can be verified by transforming S-domain closed loop transfer function to Z-domain[4].

V. MATLAB SIMULATION AND RESULTS

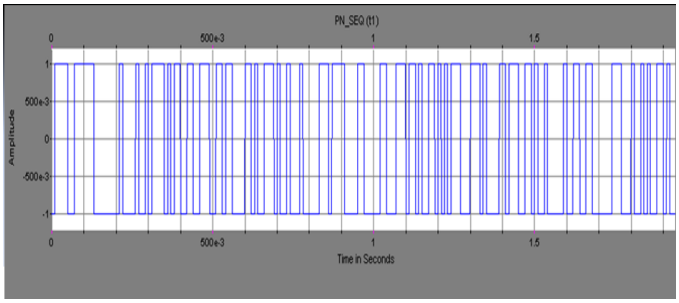

Figure 9: PN Sequence

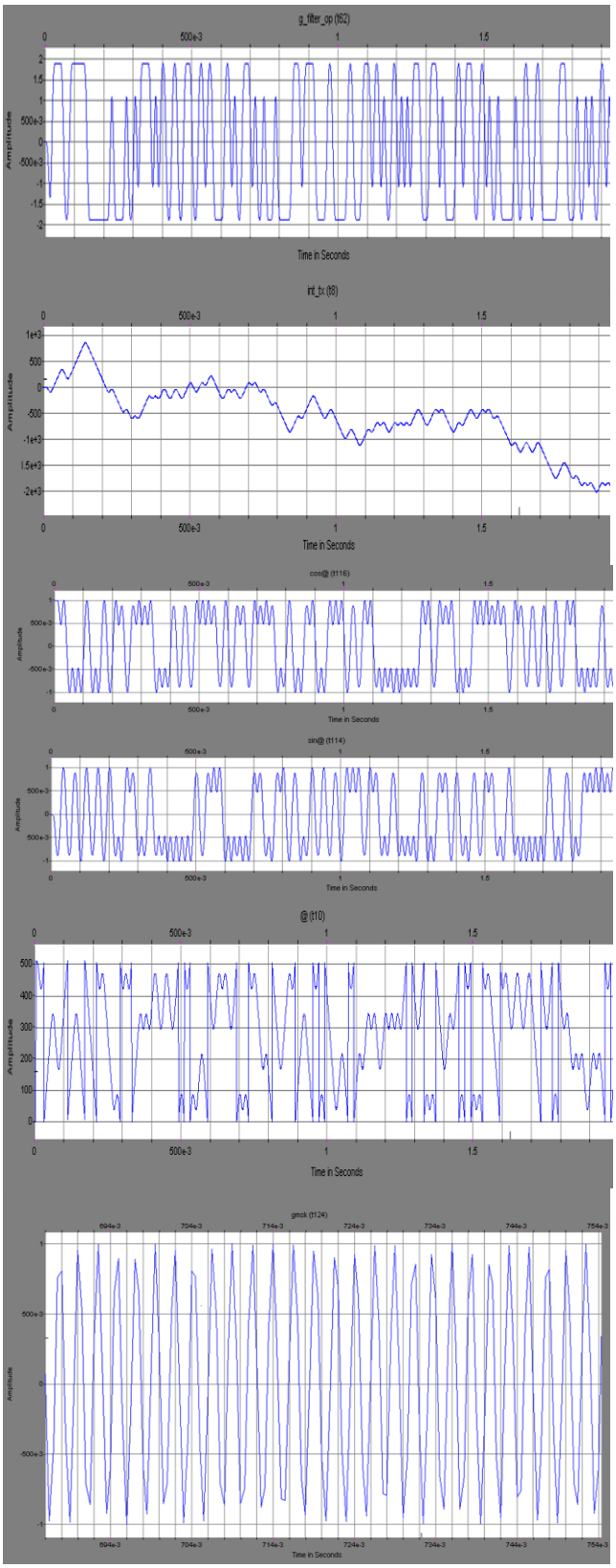

Figure 10: Gaussian Filtered o/p, Integrated o/p, Wrapped Phase I and Q Components, GMSK Signal

Figure 9 is the PN sequence which is in the form of bipolar format. 10 is the Gaussian filtered PN Sequence followed by the phase accumulation. Wrapping of the phase is performed so that phase change is continuous and the GMSK signal is obtained by adding In-phase and Q-phase Components which gives a continuous phase modulated signal.

VI. FPGA Implementation and Results

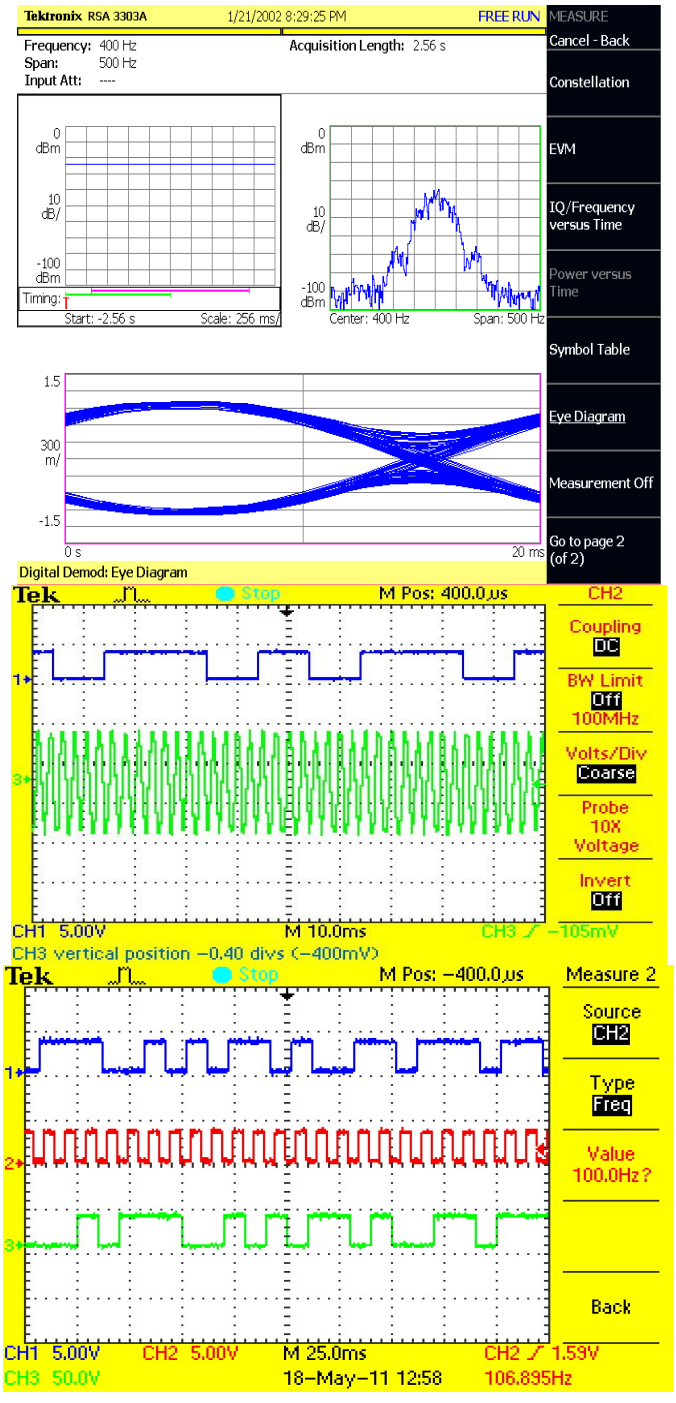

Figure 11: (a) GMSK Power Spectrum and Eye Diagram, (b) PN Sequence and GMSK Signal, (c) Received PN Sequence and Recovered Clock

Xilinx ISE and QuestaSim tools are used for implementing the design in FPGA. After generating bit file for the Digital receiver Algorithm top level design it is downloaded to Virtex-4 XC4VSX35-10FF669 Xilinx FPGA embedded in the Xtreme DSP Development Kit IV. It has one main User FPGA 4 XC4VSX35-10FF669 with 3 million gate capacity. It is used for user design. It has one Clock FPGA Virtex-II XC2V90-4CS144. This FPGA is used for the clock distribution to User FPGA.

VII. Conclusion

The top level design of the GMSK Demodulator is synthesized and post synthesis simulation, placement, layout and routing of the top level design was completed and programming file was created. The programming file was loaded into the Virtex-4 XC4VSX35-10FF669 FPGA embedded in Xtreme DSP Development Kit IV and real time testing is carried out. The in-built Demodulation algorithms available in Spectrum analyzer, was used as a part of real-time testing of the GMSK Demodulator and it was verified that proper demodulation is possible from the modulated data and all the test results are found to be satisfactory.

The GMSK Demodulator is implemented and real time testing is carried out under ideal conditions of BT product of 0.5 and without noise. The performance analysis of GMSK Demodulator with BT product less than 0.5 and noisy environment is to be carried out in real time. In order to ascertain the performance, adaptive equalizer can be built and Laurent Decomposition method can be implemented as a future work.

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