Digital Implementation of Efficient Low-Power and Compact Codec System for Portable Devices Using CADENCE Tool

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Abstract--- Power, area, timing these three characteristics are very important in the design of low power VLSI systems, especially in the multimedia applications and portable devices like hearing aids, mobiles, personal digital assistants are running with battery. In the early complex designs, to achieve power and area a conventional codec design has become a major problem in the portable device which consumes more amount power and larger area. One of the mode to take this power and area problem in the portable applications is to design very optimized low power, area, a novel CODEC Design implemented using the bus Berger inverter codec specially for running with battery based portable devices. This paper suggests a CODEC system of the Berger-invert codes and a new system of encoding/decoding circuitry (a codec). Physical layout execution results prove that the new optimization design reduces the codec area and power consumption respectively by up to 15% and 33% for different bus widths. Simulations and synthesis are carried out from different tools to select the vital design factors are presented. Accordingly, to measure critical specifications of the CODEC circuit, Two variations of digital coding, encoding & decoding circuit with many transistors are fabricated. The measurement results bring out the different low power and area possibilities as well as the developed a sophisticated digital Verilog description language for encoding decoding advanced design for the object applications. The useable SOC Encounter tools offer optimized physical layout design fabricated with 65nm and 45nm technology with comparison for CODEC with limited power, area and timing which will useful for the portable devices.

Keywords--- CODEC, Berger Invert Code, SOC Encounter Tool, Synthesis, Digital Physical Layout.

I. INTRODUCTION

THE supporting of battery based portable multimedia systems in our daily life is dramatically increasing. Some new stimulating applications, in addition to the increased care to multimedia applications, have great interest on battery-furnished, low power wireless CODEC systems. Therefore, these systems demand to be modest, low cost and have a

moderately battery lifetime, i.e. operate in an extremely limited power and area. Such systems need to innovate outstanding challenges entire end-to-end, the design system process. While high data rates are not necessary in most situations, holding communication systems and portable device reliability under low power and area operation is difficult.

In the present VLSI system design tremendous changes, especially in the field of emergency battery based system applications like multimedia, wireless communication systems, computer networks, home and business applications, have gained a steep development in the early days. One of the significant elements in the extensive dispersed of these systems is low power and area [1]. In such battery based systems due to technology scaling, power and area and timing become essential. A low power CODEC system plays a significant part of the running portable battery based system. It raises synchronization in between an encoder and a decoder with high speed by utilizing all the bandwidth.

A battery-operated based VLSI system has only confined power. But some of the portable multimedia systems are running with more power so this design is totally impossible. Therefore, the above application to stand high-computation a combined encoder and decoder (CODEC) system required to reduce power and area, the new CODEC system design must run with low-power design [3]. Low-power area techniques generally employed in algorithm, architecture and system stages. The main logic is to have a CODEC design that has less power consumption ways.

In communication and multimedia devices a codec plays significant role by encoding and decoding the larger files such as video and audio files. Hence to design an efficient codec we need to meet the two major constraints in VLSI i.e. power and area. A Bus-Invert technique [2] is used to meet the challenges that are faced during the power reduction scheme in a codec. In Bus-Invert technique, power utilized by the codec is reduced by reducing the rate of switching transitions occurred in information byte. The number of transitions in a byte of information are measured and inverted and encoded.

Simulation and synthesis results are very important in the design of encoder and decoder circuits will give idea for real time fabrication which is useful in various applications. Even for before going for real time fabrication if we very the synthesis result we will get complete idea about our designs so that it is possible to do some modification to meet proper design. The present paper we developed and tested different

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type of encoder and decoder sub circuits for battery based multimedia application

II. CODEC SIMULATION

The simulation of the combined codec(encoder decoder) circuit design was completed cadence launch is the sub tool used for simulation and behavior of the VHDL code verified. The final simulation results and behavior from the VHDL simulated 64 BIT was shown in the below. Anyway, the present design is more efficient than existing results and based on that next step synthesis implementation done perfectly with 45nm technology.

III. SYNTHESIS AND SCHEMATIC GENERATION

The present combined CODEC (encoder and decoder) design, simulation results verified from different tools like Xilinx, cadence after defensible simulation with different data bits like 32 and 64 bits with the different behavior of the simulation. The digital process used in this project, the synthesis tool was a Design Cadence GUI tool. To obtain the synthesis results, first we developed VHDL code for encoder and decoder then implemented combined as CODEC top level circuit. The synthesis results are very important to carry out the physical layout of the design and which will give the complete details about power and area and timing based on that real time digital fabrication process will be developed. In the synthesis process the developed VHDL code would be converted in to logic gates or the hardware module of the design for further implementation. To carry out the synthesis use the basic procedure and the results are shown in the table.

Figure 1: Synthesis Result of 64 bit Encoder

SNO	PARAMETER	VALUE
1	Area	891 μm^2
	Total die area	1500 μm^2
2	Cell and fill area	422 μm^2
3	Cell area	398 μm^2
4	Number of cells	6745
5	Parasitic(total capacitance)	1000pf
6	Leakage power	879.533nw
6	Estimated dynamic power (100MHZ)	2080096.406nw
7	Total power	1595026.486nw
8	Timing	7221ps

Figure 2: Synthesis Result of 64 bit Decoder

Figure 3: Synthesis Result of CODEC 64 bit Decoder

Table 1: Power and Area Result of 64 bit Encoder & Decoder for 45nm Technology

Name of the Module	Power (nw)	Area(μm^2)
Encoder	362858.23	3409
Decoder	329592.263	3237

Table 2: Power and Area Result of 64 bit Encoder & Decoder for 65nm Technology

Name of the Module	Power (nw)	Area(μm^2)
Encoder	474625.33	4215
Decoder	358542.713	3628

IV. PHYSICAL LAYOUT

The Digital physical layout of the CODEC circuit block was designed using a SOC Encounter Cadence tool using 45nm technology. To start this process, all arrangements and input files should first be added into the search tool. In the GUI graphical user interface, a plain chip of the correct size with different views and external power rails must be defined properly. The present CODEC design, the rails is laid out to be 15 microns wide in metals 1 and 2 for least via losses, but it is the general way to prefer in review to take metals 5 and 6 for moderate conductivity. Internal power rails are added for carrying each of the separate cells.

On this CODEC circuit defining power and ground for encoder and decoder also challenge task to carry out complete physical design for that, after adding power supply, the pins were arranged around that outer side of the chip with their placement based on codec functionality. The encoder data input and output bus width lines are carefully placed in order

to transfer the information from the encoder to decoder were placed on the upper and lower respectively. The digital physical layout process starts with floor planning and finish with post routing. The complete process around forty two steps to design the complete 64 bit CODEC digital physical

layout. Finally we have investigated from our design with different parameters to minimize the power, area and timing for battery based devices in multimedia applications and these results are shown in the table.

Power Planning

Placement and Routing

Final CODEC Digital Physical Layout for I=64 BIT

Table-2 Synthesis of CODEC Physical Layout Results Implemented in SOC Encounter Tool.

V. CONCLUSION

The CODEC designed work has been successfully implemented with the SOC Encounter tools with 45nm technology of digital physical layout and the operation of encoding and decoding the data from VHDL code level data, to gate level and transistor level implementation, synthesis results with design metrics like power, area and timing carried out and compared with existing designs. Finally a digital physical layout which includes floor planning and power and routing and final CODEC physical layout implemented and for future fabrication and chip for final real time results. Especially in this paper CODEC circuit having ultra low power, minimum area and optimized timing are used for battery based applications. The present design 64 bit CODEC can be extended to a 128bit CODEC by modifying the vhd code with additional libraries.

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TECHNOLOGY.

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